# Asymmetrical Extended Min-Sum Successive Cancellation Decoder


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This work has been partially funded by the French ANR under grant number ANR-19-CE25-0013-01 and the Lebanese International University.

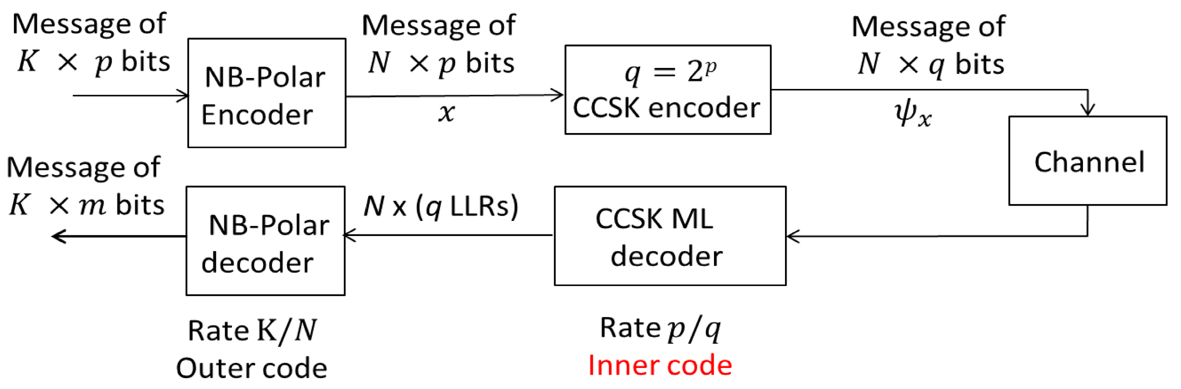

## Non-Binary Error Correction Codes and CCSK Modulation

- Non-Binary (NB)-Error Correction Codes have high error correction capability even over short Frames. When associated to Cyclic Code-Shift Keying (CCSK) modulation, NB codes enables ultra-low power transmission.

This paper considers the latest capacity-approaching error-correcting codes which are the Polar codes, and specifically their NB family:
- Complexity reduction by a factor of 2 is obtained.
- Performance loss of 0.15 dB is observed over AWGN CCSK modulated channel.

## Cyclic-Code Shift Keying

The Cyclic-Code Shift Keying (CCSK) modulation is a modulation technique based on the spread-spectrum modulation, where a message of size $p$-bits represented in decimal as $\alpha \in GF(q = 2^p)$ is modulated over a Pseudo-random Noise (PN) sequence of size $q$.




Assume PN sequence for $q = 8$, $P$ = 11101000.
CCSK modulation: $\psi_{x_i} = rot(P, x_i)$ (right circular rotation of $a$ position)

Assume $x = (x_0, x_1, x_2, x_3) = ((011)_2, (001)_2, (100)_2, (110)_2)$
Transform to decimal values: $x = (3,1,4,6)$.

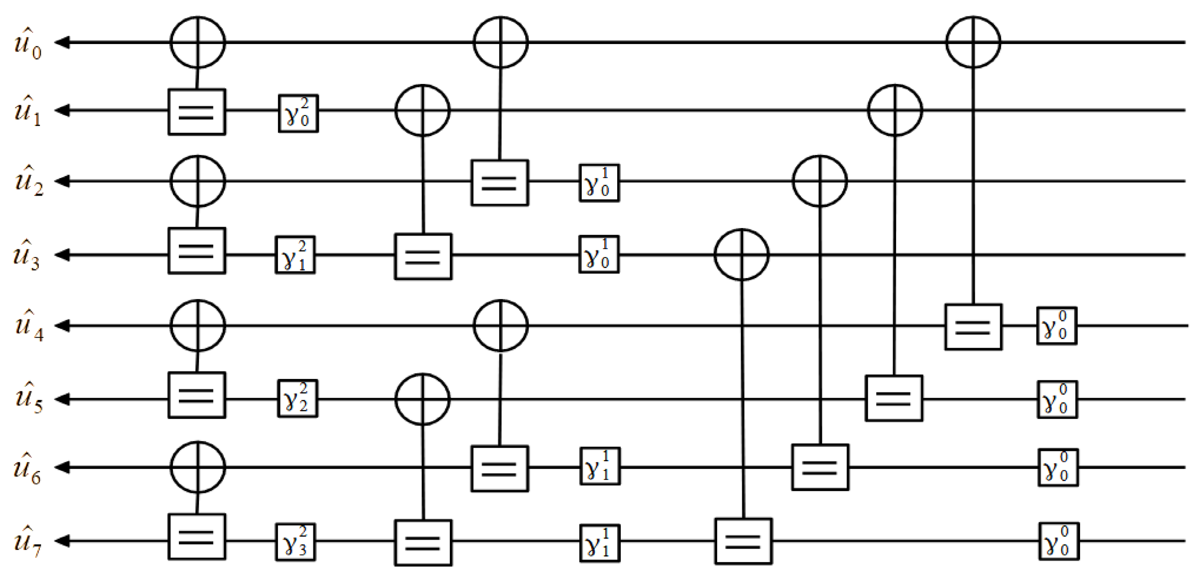
Associate CCSK symbol: $rot(P,3)$ & $rot(P,1)$& $rot(P,4)$&$rot(P,6)$
$\psi_x$ = ("00011101", "01110100", "10001110", "10100011")

## Polar Codes and Decoders

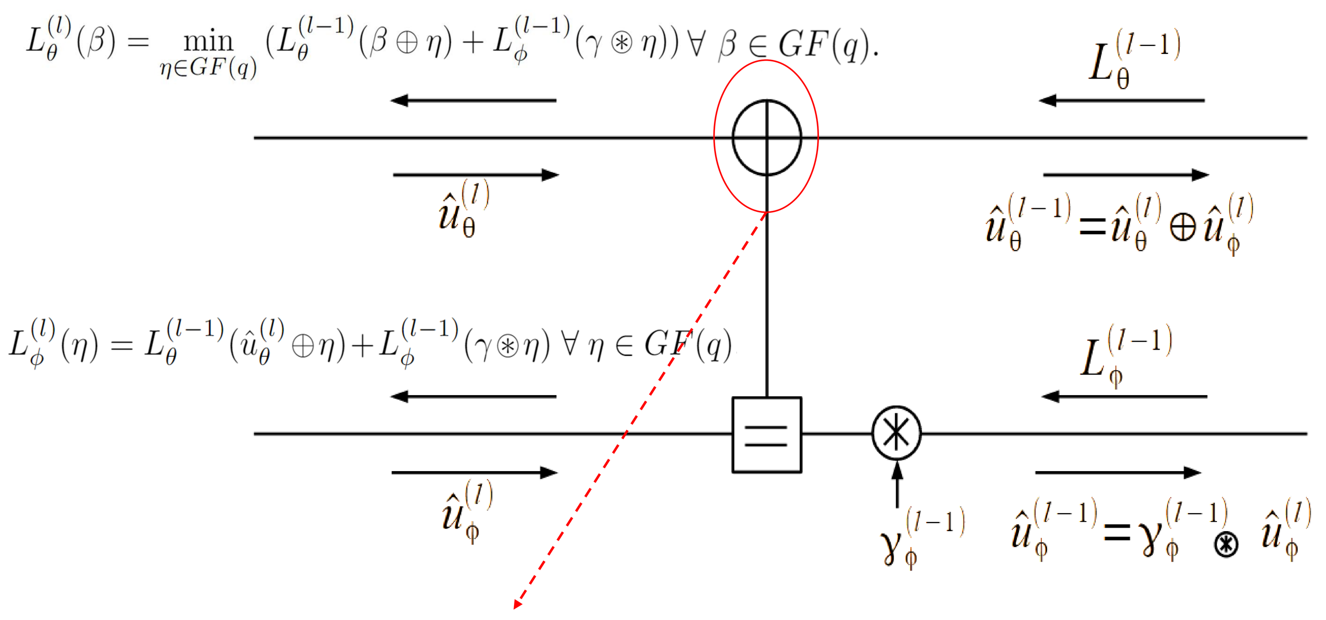
The kernel $G_2$ transforms the input vector $u = (u_0, u_1)$ into an output $x = (x_0, x_1)$ by the following input-output relation

$$G_2 = \begin{bmatrix} 1 & 0 \\ 1 & \gamma \end{bmatrix}, \ \gamma \in GF(q). \qquad \begin{cases} x_0 = u_0 \oplus u_1 \\ x_1 = \gamma \circledast u_1 \end{cases}$$

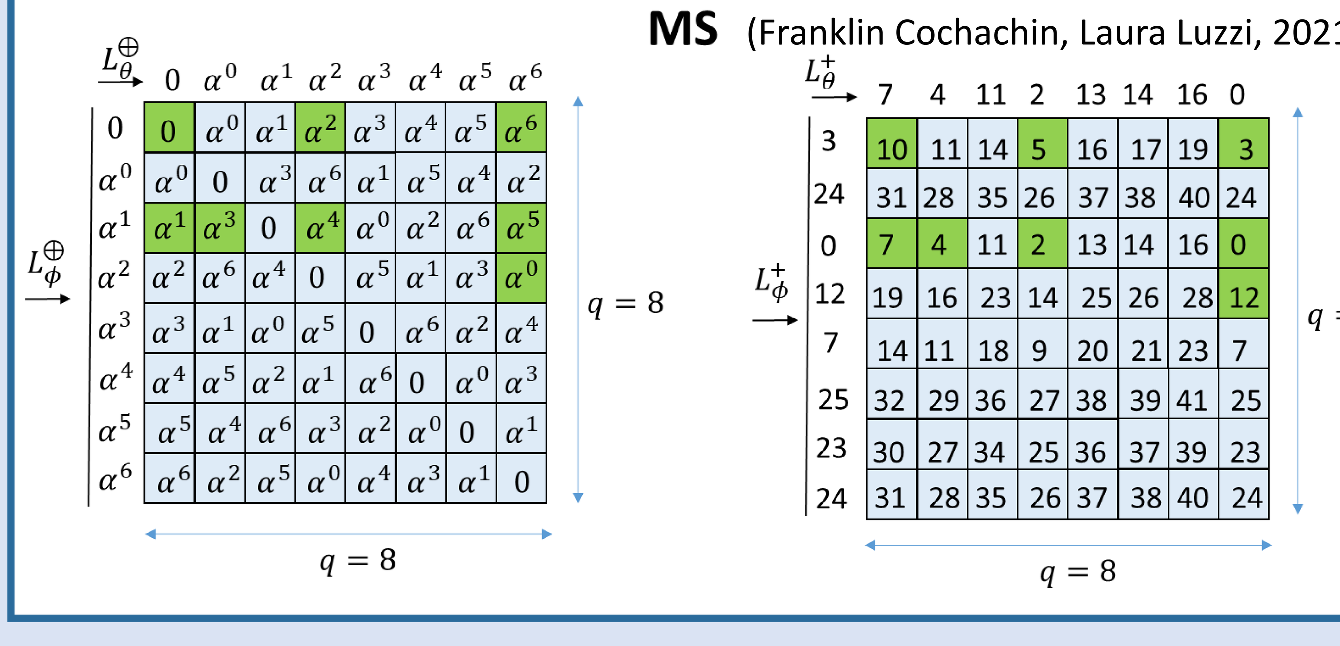
### Polar Decoder for $N = 8$.



### Message Propagation of Kernel Decoding




**MS** (Franklin Cochachin, Laura Luzzi, 2021)



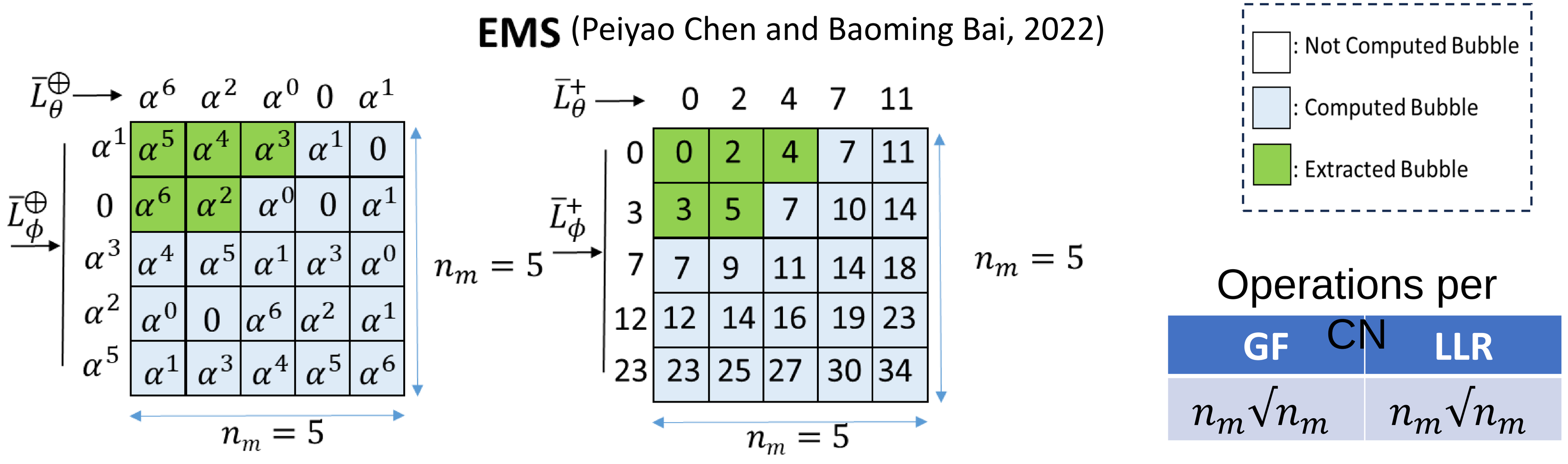
Operations per CN

| GF | LLR |
|---|---|
| $q^2$ | $q^2$ |

## Asymmetrical Extended-Min Sum SC Decoder

Computed Region in Different Check Node Algorithms: Toy Example on GF(8)

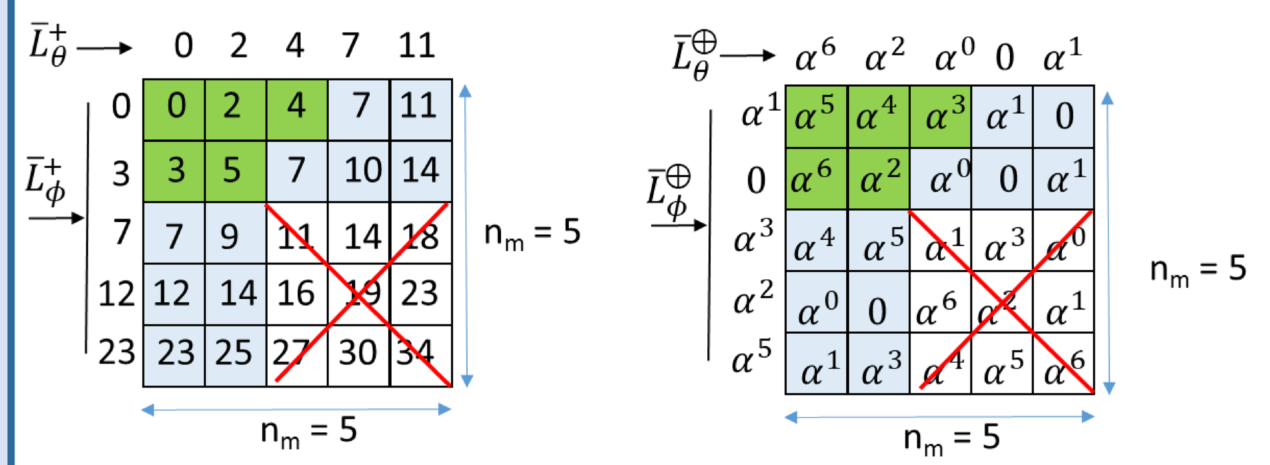
**EMS** (Peiyao Chen and Baoming Bai, 2022)




Operations per CN

| GF | LLR |
|---|---|
| $n_m\sqrt{n_m}$ | $n_m\sqrt{n_m}$ |

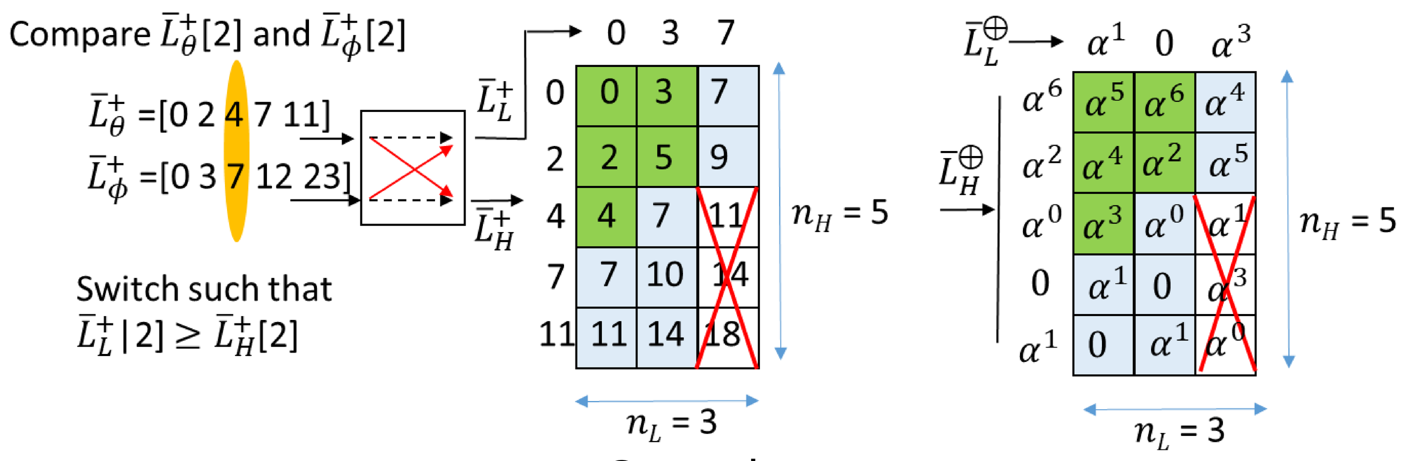
**LEMS** (Emmanuel Boutillon and Laura Conde-Canencia, 2010).



Operations per CN

| GF | LLR |
|---|---|
| $4n_m - 4$ | $2n_m - 3$ |

**Proposed AEMS**




Operations per CN

| GF | LLR |
|---|---|
| $2(n_L + n_H) - 4$ | $(n_L + n_H) - 3$ |

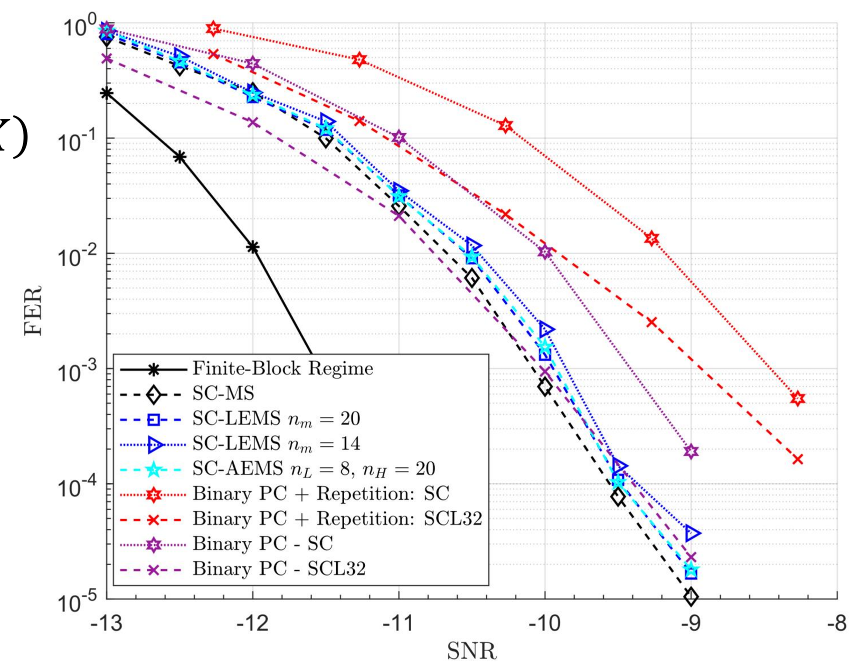
## Complexity Analysis and Simulation Results

NB-PC with $\gamma = 1$ (Cochachin, Ghaffari , 2023)

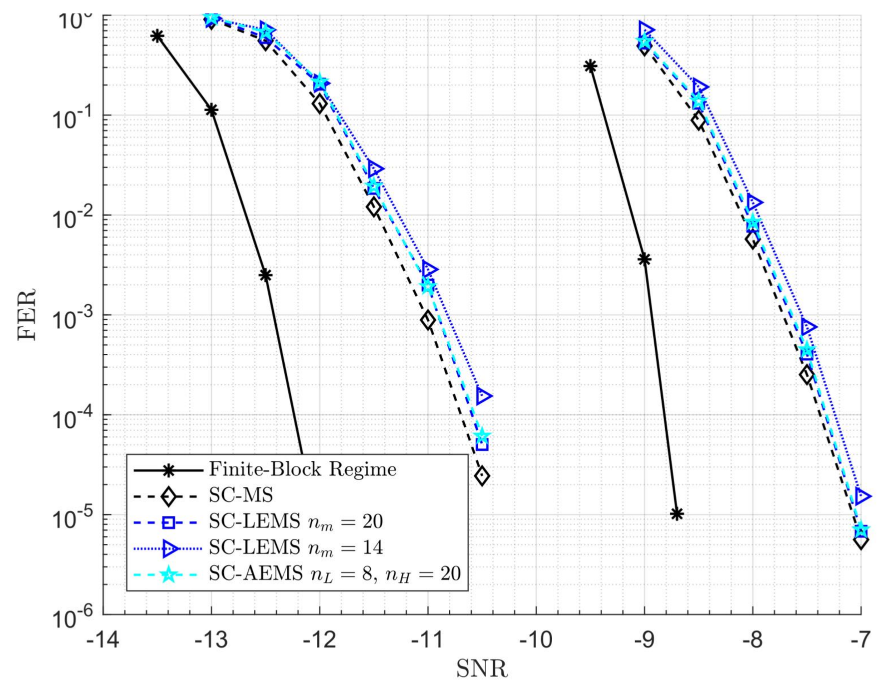
Simulation Result on GF(64) with $(K, N) = (21,64)$ $(PC\ GF(64) + CCSK)$ $= (126, 4096)$ (binary)
$r$ = 21/64 × 6/64 = 0.0308

Equivalent binary polar code $(K, N)$ =(126, 4096), $r$ = 0.0308

Binary polar code + repetition (126, 384) + ~10.7 repetitions (like 5G-NB standard). Overall code rate: 0.0308.




Simulation Result on GF(64) with $K = 42$ (left), $K = 85$ (right) and $N = 256$.




## Conclusion and Future Work

- Proposition of AEMS algorithm to **reduce check node complexity**: Applying/adapting L-bubble and pre-sorting (developed for NB-LDPC decoder) to the check node kernel with **Small performance degradation** (<0.15 dB).
- **Similar performance than SCL-32 binary polar code!**
- Future work: customize each check node of the graph to further reduce the overall complexity. **Very promising preliminary results**.